Remarks

Reconsideration of the above referenced application in view of the enclosed amendment and remarks is requested. Claims 1-38 stand rejected. Claims 9, 19, 29 and 34 have been amended to overcome the § 112 rejection. Claims 9, 19, 29 and 34 have been amended to recite "one or more second devices" to overcome any issues with antecedent basis. Claims 1 to 38 are pending in the application.

ARGUMENT

Claims 9-10, 19-20, 29-30 and 34 are rejected under 35 U.S.C. § 112, second paragraph. This rejection is moot based on the foregoing amendments and following discussion. Claims 9, 19, 29 and 34 have been amended to reference "the one or more second devices," as recited in the parent claims, thereby nullifying the Examiner's rejection based on antecedent basis.

Claims 1-7, 9-17, 19-27 and 29-34 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Dent et al., (U.S. Pat. 5,598,575) (hereafter, "Dent et al."). This rejection is respectfully traversed and Claims 1-7, 9-17, 19-27 and 29-34 and 38 are believed allowable as amended based on the foregoing and following discussion.

Dent et al. teach a system including a control processor, a coprocessor, a program memory and a data memory, where the control processor accesses the program memory during an instruction fetch cycle and the data memory during an instruction execution cycle. The apparatus taught by Dent et al. uses a direct memory address (DMA) controller to control access to the memory by a control processor and one or more coprocessors. (See Fig. 1, items 5, 6, 7, 8, and 11-16) Figure 1 of the reference clearly shows the connectivity of components. Figure 2, as cited by the Examiner, provides further detail of the DMA controller 6, and fails to show alternative connections between the host processor 5 and other components, such as memory 7, 8. It is clear that Dent et al. teach a system where the host processor does not have direct access, i.e., is not connected, to memory components via a bus. Col. 10, lines 31-34 explicitly teach that "the control processor 5, which is for example a ZILOG Z80 having a Von Neumann type of architecture, has a single address bus and bidirectional data bus connection to the DMA

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controller 6 ." [Emphasis added] All memory accesses are controlled by the DMA controller. Dent at al. do not teach that the control processor (host) is connected to one or more second devices, e.g., memory devices, via a signal line, or bus. Instead Dent et al. teach a system where the control processor (host) is connected to the DMA controller via a data and address bus. This is in contrast to Applicant's claimed invention.

Applicant recites a system where the host processor (Fig. 2, 208) is connected to a bus switch 212 and memory modules 204 (second devices) via a bus 206. The first device (FGPA 202) has access to data on the bus 206 via a tap line 215. Thus, the host processor 208 can access memory modules 204 simultaneously while the FGPA 202 accesses the SDRAM 210. Specifically, at a given point in time, if the bus switch connects the FGPA 202 and the SDRAM 210, the host 208 has full access to the memory modules 204 without requiring waiting for any aspect of the instruction fetch cycle, as taught by Dent et al. Further, Dent et al. do not teach or suggest a tap line to an existing bus, but instead completely traps and controls all address communication from the control processor (5) and coprocessors (11-16). The coprocessors 11-16, which the Examiner likens to Applicant's FGPA 202 have no direct connection, or tap line, to the address bus used by the control processor 5. Instead, Dent et al. teaches that any information sent by the control processor or co-processors to a bus is trapped, analyzed, and perhaps transformed, by the DMA controller before it is sent to a memory device.

Moreover, Dent et al. teach a system where "after a Direct Memory Access scheduler has served this number of data memory accesses, it ceases to access the data memory in time for the control processor to assert, if needed, the switch control signal that reconnects the RAM bus to the control processor." This operation is in contrast to Applicant's claimed invention. The switch in Applicant's invention is controlled by the first device (FGPA 202) and not the host processor 208. For instance, as recited in independent Claims 1, 11, 21, and 31 a switch event *is initiated upon detection, by said first device, of a predetermined sequence of data values on the tap line, and wherein said event selectively switches a communication path from a third device to one of said host and said first device.* At no time does the host processor of Applicant's recited invention assert the switch control signal, as taught by Dent et al.

Further, with regard to Claims, 9, 19, 29, 34 Applicant's recited invention requires that *each of the plurality of data values represents a memory location within any of the one or more*

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second device. Applicant recites that when a memory sequence is sent to initiate the switch between the host and first device, that the data memory locations can be within any of the memory devices 204. In other words, in a three address sequence, the first and third memory addresses may be in memory device A and the second address location may be in memory device B, as described in the specification on page 9, line 18 through page 10, line 6. In contrast, the system taught by Dent et al. requires that a single memory address and a read indicator identify that the bus line should be switched between the control processor and coprocessors. Dent et al. do not teach a sequence of memory addresses indicating that the bus line should be switched between the host processor and the first device (FGPA), where the addresses are captured via the tap line. Thus, the Examiner has failed to show all of the recited elements in the cited reference.

Claims 8, 18, 28 and 35-37 are rejected under U.S.C. § 103(a) as being unpatentable over Dent et al. in view of "what is well known in the art." This rejection is respectively traversed and Claims 8, 18, 28 and 35-37 are believed allowable based on the foregoing discussion. This rejection is moot based on independent Claims 1, 11, 21, and 31 being allowable. All pending claims are therefore in condition for allowance.

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CONCLUSION

In view of the foregoing, claims 1-38 are all in condition for allowance. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (703) 633-6845. Early issuance of Notice of Allowance is respectfully requested. Please charge any shortage of fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0221 and please credit any excess fees to such account.

Respectfully submitted,

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